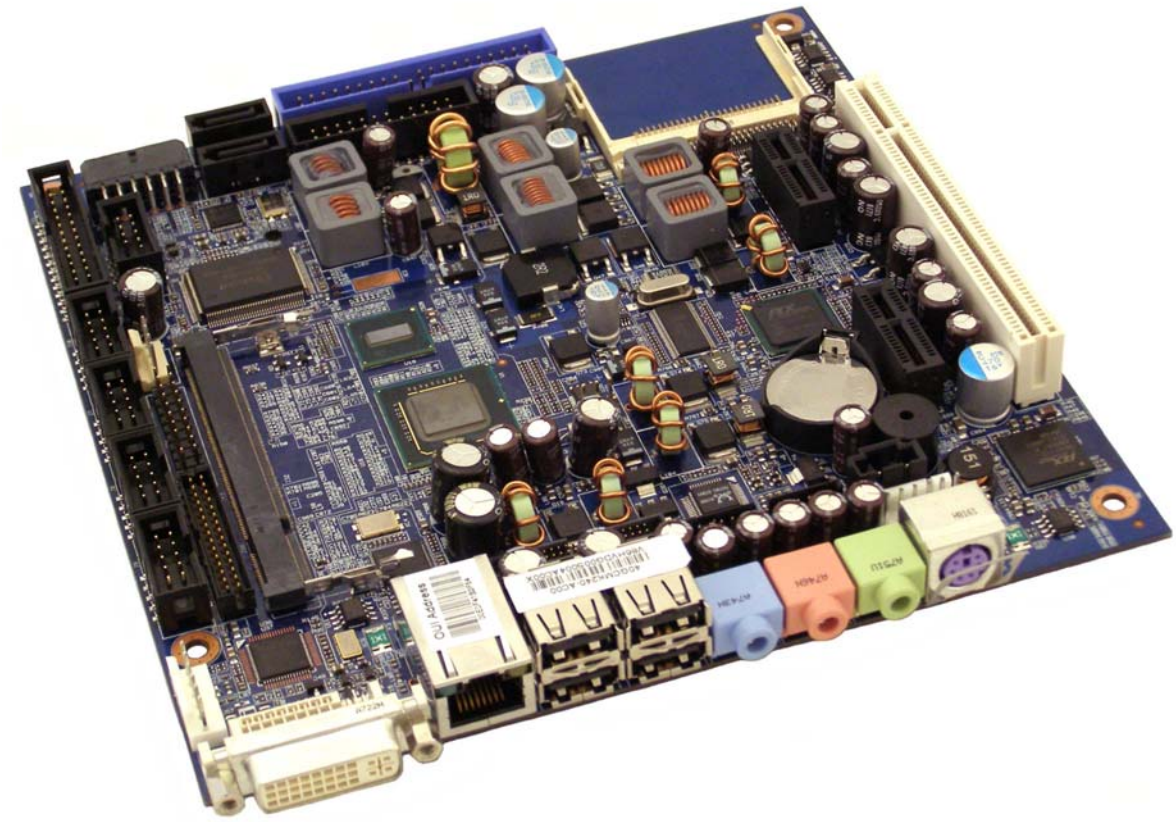
User Manual

for the Motherboards:

KTUS15/mITX Board Family



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- CPU Board
  1. Type.
  2. Part-number.
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Introduction

This manual describes the KTUS15/mITX boards made by KONTRON Technology A/S. The boards will also be denoted KTUS15 family if no differentiation is required.

The boards use the Dual-Core Intel® Atom™ processor together with the Intel® US15W chipset.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTUS15/mITX Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 2 before switching-on the power.

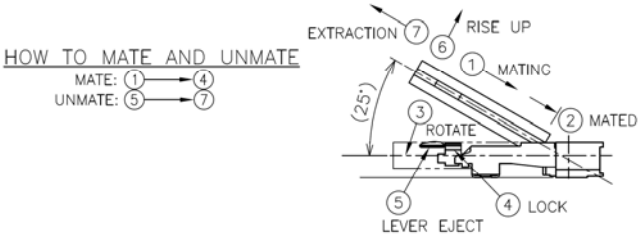
2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has DDR2 DRAM mounted. In this case Step 2 can be skipped.

1. **Turn off the power supply**

2. **Insert the DDR2 SODIMM 200pin DRAM module**
   See guidelines below for assembling / disassembling memory module.
   For a list of approved DDR2 DIMM modules contact your Distributor or FAE.
   DDR2-400 and DDR2-533 SODIMM 200pin DRAM modules (PC3200, PC4200) are supported.



3. **Connecting Interfaces**
   Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings to flat panel support.

4. **Connect Power supply**
   Connect power supply to the board by the 6x2pin PWR connector. NOTE: the board is a single-supply board, accepting input voltages from 5V to 25V (DC). Power cables for connecting the KTUS15 family boards to a ATX power supply (+5V or +12V) is available from Kontron (P/N 1022-6309).

5. **Turn on the power on the power supply**

6. **Power Button**
   The PWRBTN_IN may be required to start the board; this is done by connecting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description) to provide a pulse on the PWRBTN_IN pin. A “normally open” switch can be connected via the FRONTPNL connector.

7. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up. Refer to the “BIOS Configuration / Setup“ section of this manual for details on BIOS setup.

Note: To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with or without power) for approximately 1 minute. This will also disable any Secure CMOS setup on the board.
Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

2.2 Requirement according to EN60950

Users of KTUS15 family boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarises the features of the KTUS15/mITX embedded motherboards.

Form factor	KTUS15/mITX: mini ITX (170.18millimeters by 170.18millimeters)
Processor	• Intel® Atom™ BGA processors 1.1GHz (Z510) or 1.6GHz (Z530) depending on board configuration. • On die, primary 32-kB instructions cache, 24-kB write-back data cache, and 512-kB, 8-way L2 cache. • 533-MHz (Z530) / 400-MHz (Z510) Source-Synchronous front side bus speed (FSB) • Supports Hyper-Threading Technology 2-threads (Z530 only) • Supports C0/C1(e)/C2(e)/C4(e) and Intel® Deep Power-Down Technology (C6) (C6 support Z530 only) • Thermal Design Power (TDP) of 2W for Intel® Atom™ processors Z510 and Z530
Memory	• DDR2 SODIMM 200pin DRAM socket • Supports 1.8-V DDR2 SDRAM • Supports 400 MT/s and 533 MT/s data rates • Support system memory from 512MB and up to 2GB (* to be confirmed) • ECC not supported
Chipset	• Intel® System Controller Hub US15W
Video	• Intel® Graphics Media Accelerator 500 • Ultra Low Power Integrated 3D Graphics core • Graphics controller core frequency of 200MHz • Full hardware acceleration of video decode standards, such as H.264, MPEG2, MPEG4, VC1, and WMV9 • Video memory up to 256MB • Analog Display CRT output (depending on configuration) with support for analogue monitors up to 1600x1200 at 60Hz. • Digital Visual Interface digital outout (DVI-D) (depending on configuration) with support for digital monitors up to 1600x1200 at 60Hz. • Single channel 18/ 24bit LVDS panel support (OpenLDI/ SPWG) up to Wide XGA (1366x768 @ 85Hz) panel resolution. With external 1-to-2 pixel per clock converter, LVDS panels up to 1280x1024 are supported. • Dual independent pipe support, Mirror and Dual independent display support.
Audio	Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the Realtek ALC888 codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1, MIC2 • CDROM in • SPDIF Interface Onboard speaker

(continues)

I/O Control	Winbond W83627DHG LPC Bus I/O Controller
Peripheral interfaces	• Four USB 2.0 ports on I/O area • Four USB 2.0 ports on internal pinrows • Two / Four Serial ports (RS232C) (depending on board configuration) • One Parallel port, SPP/EPP/ECP • Two Serial ATA-150/300 IDE AHCI (depending on board configuration), RAID not supported. • One PATA 33/66/100 interface with support for 2 devices • CF (Compact Flash) interface supporting CF type I and II. (UDMA2 max.). Note that only one PATA device is supported when CF is used and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA devices. • PS/2 keyboard and mouse ports
LAN Support	• 10/100/1000Mbits/s LAN using Intel ® 82574L controllers • RPL/PXE netboot supported. Wake On LAN (WOL) supported (S3 only).

BIOS	• Kontron Technology / AMI BIOS (core version 8.00)
	• Support for Advanced Configuration and Power Interface (ACPI 3.0), Plug and Play
	  ○ Suspend To Ram
	  ○ Suspend To Disk
	  ○ Intel Speed Step
	• Secure CMOS/ OEM Setup Defaults
	• “Always On” BIOS power setting
	• System Locked Pre-Activation (SLP) key support
	• Boot-Logo / Long splash support
	• Setup for Forced Boot device
	• Desktop Management Interface (DMI) with user-configurable setup
	• TPM version 1.2 support

Expansion Capabilities	• PCI Bus routed to 1 PCI slot (PCI Local Bus Specification Revision 2.3) • PCI-Express bus routed to 2 (x1)PCI Express slots (PCI Express 1.0a) • Two Secure Digital I/O (SDIO) card slots (backside) • SMBus routed to TPM header, Feature connector, PCI, and PCI Express Slot connectors • LPC Bus routed to TPM connector • DDC Bus routed to LVDS and CRT /DVI connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for two onboard Fan control connectors: FAN_CPU and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3ºC) • Voltage monitoring • Intrusion detect input • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• WinXP Professional • Windows Vista • WinXP Embedded (limitations may apply) • Linux: Feodora Core 10, Suse 11.1 (limitations may apply)

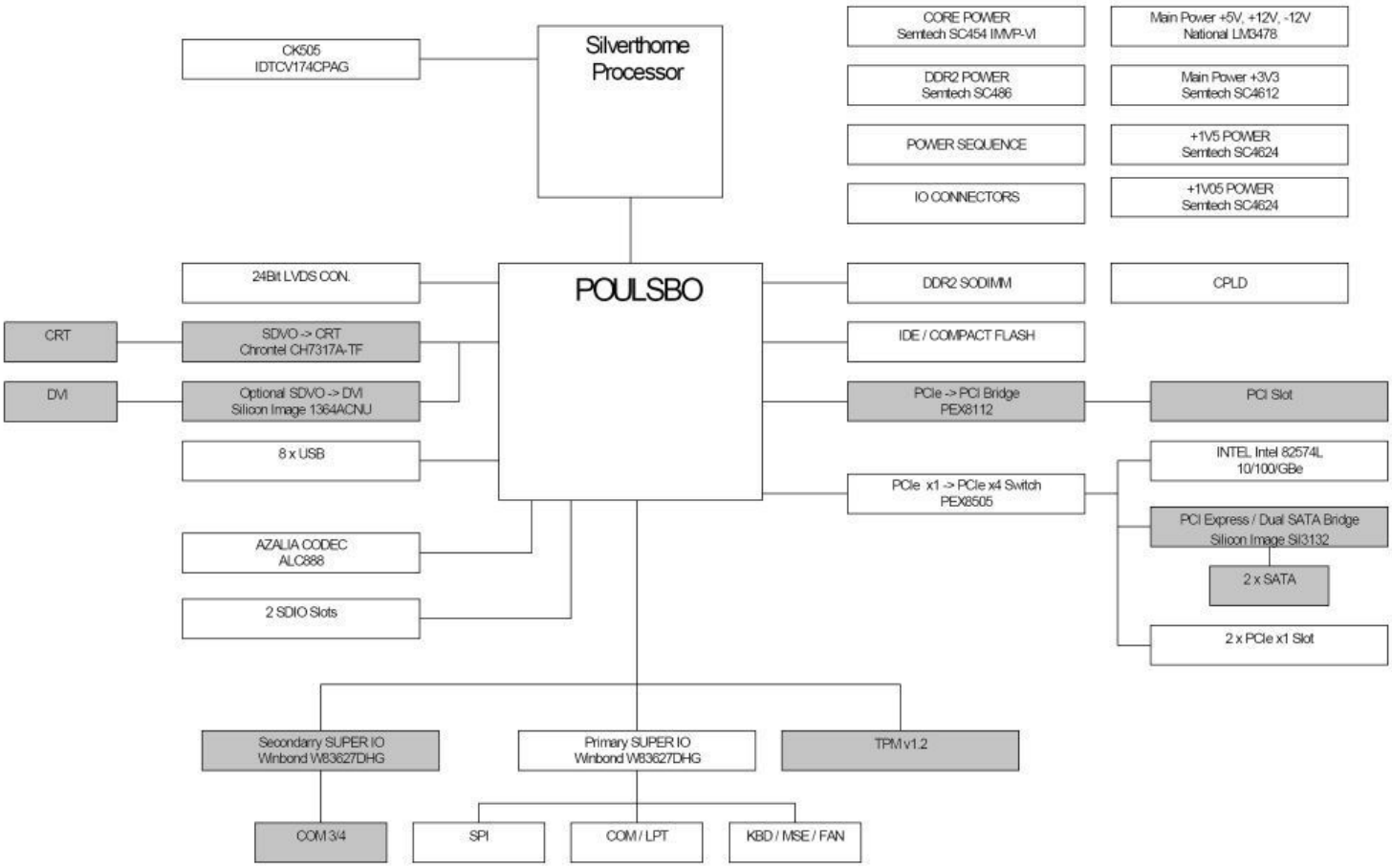
(continues)

Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition, **Approval pending** CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** TBD **Restriction of Hazardeous Substances (RoHS):** All boards in the KTUS15 board family are RoHS compliant. **Capacitor utilization:** No Tantal capacitors on board Only Japanese brand Aluminium capacitors rated for 100degrees Celsius used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / PN CR2032NL/LE or CR-2032L/BE. Expected minimum 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 3-4 µA (no PSU connected). **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 System overview

The block diagram below shows the architecture and main components of the KTUS15 family boards.

Components shown shaded are optional depending on variants of the board.



3.3 KTUS15/mITX Board configurations

	P/N 810290 KTUS15/mITX 1.6GHz Std	P/N 810291 KTUS15/mITX 1.1GHz Basic	P/N 810292 KTUS15/mITX 1.6GHz Plus	P/N 810293 KTUS15/mITX 1.1GHz Std
Processor	Z530, 1.6GHz	Z510, 1.1GHz	Z530, 1.6GHz	Z510, 1.1GHz
FSB speed	533MHz	400MHz	533MHz	400MHz
Memory, DDR2 SODIMM	Up to 2GB (TBD)	Up to 2GB (TBD)	Up to 2GB (TBD)	Up to 2GB (TBD)
Video output				
CRT (DVI-A)	Yes	No	No	Yes
DVI (DVI-D)	No	Yes	Yes	No
LVDS	Yes	Yes	Yes	Yes
LAN	Yes	Yes	Yes	Yes
HD Audio	Yes	Yes	Yes	Yes
SATA port	Yes, 2 ports	No	Yes, 2 ports	Yes, 2 ports
PATA port	Yes, 1 port	Yes, 1 port	Yes, 1 port	Yes, 1 port
Compact Flash slot	Yes	Yes	Yes	Yes
SDIO slot	Yes, 2 slots	Yes, 2 slots	Yes, 2 slots	Yes, 2 slots
USB port	Yes, 8 ports	Yes, 8 ports	Yes, 8 ports	Yes, 8 ports
Serial port	Yes, 2 ports	Yes, 2 ports	Yes, 4 ports	Yes, 4 ports
Parallel / Printer port	Yes, 1 port	Yes, 1 port	Yes, 1 port	Yes, 1 port
Mse / Kbd interface	Yes	Yes	Yes	Yes
Feature connector	Yes	Yes	Yes	Yes
Frontpanel connector	Yes	Yes	Yes	Yes
FAN CPU connector	Yes	Yes	Yes	Yes
PCI slot	Yes, 1 slot	No	Yes, 1 slot	Yes, 1 slot
PCI express slot	Yes, 2 PCIe x1 slots	Yes, 2 PCIe x1 slots	Yes, 2 PCIe x1 slots	Yes, 2 PCIe x1 slots
TPM chip onboard	No	No	Yes	No

3.4 System Memory support

The KTUS15 boards have one 200-pin DDR2 Small Outline Dual Inline Memory Module (SO-DIMM) socket. The socket can be populated with up to 2 GB (* to be confirmed) of unbuffered DDR2 SO-DIMM modules. Memory speeds up to 533MT/s (PC2-4200) are supported.

- Supports 1.8-V DDR2 SDRAM with gold-plated contacts
- SDRAM Organisation of x16 supported only, up to 2 ranks, 8 loads only
- Supports 400 MT/s and 533 MT/s data rates
- Single 64-bit wide single-channel
- Support system memory from 512MB and up to 2GB (* to be confirmed)
- Device density support for 512 Mb and 1024-Mb devices
- ECC not supported
- Serial Presence Detect required

The installed DDR2 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

3.4.1 Memory Operating Frequencies

The KTUS15/mITX maintains a fixed relationship between DRAM to FSB clock frequency. The FSB frequency can be 100 MHz or 133 MHz, resulting in support of the following clock frequencies and data rates for the DRAM.

CPU	FSB Speed	DRAM Clock	DRAM Data Rate	DRAM Type	Peak Bandwidth
Z510, 1.1GHz	400 MHz	200 MHz	400 MT/s	DDR2	3.2 GB/s
Z530, 1.6GHz	533 MHz	266 MHz	533 MT/s	DDR2	4.2 GB/s

3.5 KTUS15 Graphics Subsystem

The KTUS15 boards use the Intel ® US15W chipset for graphical control by the embedded Intel® Graphics Media Accelerator 500.

The Intel Graphics Media Adapter includes LVDS and Serial DVO display ports permitting simultaneous independent operation of two displays.

If external graphics is used (PCI) instead of the internal graphics device, LVDS and SDVO ports will not function.

The KTUS15 board supports a Low-Voltage Differential Signaling interface that allows the Intel Graphics Media Adapter to communicate directly to an on-board flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits, one-pixel per clock displays.

The Intel ® US15W chipset Serial DVO port either connects to a Serial DVO Digital DVI (DVI-D) or a Serial DVO Analogue DVI (DVI-A) controller depending on the board configuration (refer to KTUS15/mITX Board configurations section).

3.5.1 Intel® Graphics Media Accelerator 500

Features of the Intel® Graphics Media Accelerator 500.graphics controller includes:

- Integrated graphics (2D and 3D) and high-definition video decode capabilities with minimal power consumption
  - 200 MHz core frequency
  - UMA memory architecture.
  - Max video memory: 256MB.

- 3D Core Key Features
  - Direct3D version 10.1 and OpenGL 2.0 compliant (TBD)
  - Two pipe scaleable unified shader implementation.
    - 3D Peak Performance
    - Fill Rate: 2 Pixels per clock
    - Vertex Rate: One Triangle 15 clocks (Transform Only)
    - Vertex / Triangle Ratio average = 1 vtx/tri, peak 0.5 vtx/tri
  - Texture max size = 2048 x 2048
  - Programmable 4x multi-sampling anti-aliasing (MSAA)
  - Rotated grid
  - Optimized memory efficiency using multi-level cache architecture

- Video
  - Full hardware acceleration of video decode standards, such as H.264, MPEG2, MPEG4, VC1, and WMV9.
  - MPEG2 hardware acceleration: VLD + iDCT + MC
  - VC-1 hardware acceleration: VLD + iMDCT + MC + LDF

- Display
  - Analog Display CRT output (DVI-A) (depending on configuration) with support for analogue monitors up to 1600x1200 at 60Hz.
  - Digital Visual Interface digital outout (DVI-D) (depending on configuration) with support for digital monitors up to 1600x1200 at 60Hz.
  - Single channel 18/ 24bit LVDS panel support (OpenLDI/ SPWG) up to Wide XGA (1366x768 at 85Hz) panel resolution. With external 1-to-2 pixel per clock converter, LVDS panels up to 1280x1024 are supported.
  - Dual independent pipe support, Mirror and Dual independent display support.

3.5.2 Dual Independent / Mirror / Single Display support

The table below shows the supported display configurations for the KTUS15 boards.

Mem. Freq. 533MT/s Color depth 32bit Refresh rate 60Hz		LVDS Interface								
		No Display	640x480	800x480	800x600	1024x600	1024x768	1280x768	1366x768	1280x1024
sDVO interface	No Display	N/A	DID	DID	DID	DID	SD	SD	SD	SD
	640x480	DID	DID	DID	DID	DID				
	800x480	DID	DID	DID	DID	DID				
	800x600	DID	DID	DID	DID	DID				
	1024x600	SD								
	1024x768	SD								
	1280x768	SD								
	1366x768	SD								
	1280x1024	SD								
	1600x1200	SD								
	1600x1200	SD								

DID = Dual Independent Display / Mirror Display
SD = Single Display

3.6 KTUS15 Power

3.6.1 Power State Map

POWER NET/STATE	S0#	S3#	S5#
+VIN	ON	ON	ON
+12V_ALWAYS	ON	ON	ON
+12V	ON	OFF	OFF
-12V	ON	OFF	OFF
+5V	ON	OFF	OFF
+5V_SUS	ON	ON	OFF
+5V_ALWAYS	ON	ON	ON
+3V3	ON	OFF	OFF
+3V3_SUS	ON	ON	OFF
+3V3_ALWAYS	ON	ON	ON
+1V8_ALWAYS	ON	ON	ON
+1V8	ON	OFF	OFF
+1V8_SUS	ON	ON	OFF
+1V5	ON	OFF	OFF
+1V05	ON	OFF	OFF
+1V05_C6	ON	OFF	OFF
+0V9_SUS	ON	ON	OFF
+VCORE	ON	ON	ON
+V_BAT	ON	ON	ON

3.6.2 Power Budget

The below table shows the power budget for the KTUS15 boards. This does not reflect the actual power used.

Current Consumption	+12V	+5V	+3V3	+1V8	+1V5	+1V05	+VCORE	-12V
CPU					0.13	2.5	4	
SCH			0.14	0.6	0.87	2.5		
Memory								
Ethernet			0.67					
SuperIO								
DVI/CRT			0.11	0.3				
Audio								
FWH			0.1					
COM	0.2							0.2
PEX8505						1.2		
PEX8112			0.25					
SII3132				0.6				
USB outlet		4						
PCIe outlet	0.5		3					
PCI outlet	0.5							0.1
LVDS outlet	2.5	1.5	1					
SD outlet			0.3					
Total	3.7	5.5	5.45	1.5	1	6.2	4	0.3

3.6.3 Power Consumption

The KTUS15/mITX board is powered through the PWR connector by a single supply DC voltage between 5-25V.

The requirements to the supply voltage is as follows:

Supply	Min	Max	Note
VIN	4.75V	26.2V	Should be ±5%

Power consumption figures TBD

3.7 KTUS15 Clock Distribution

TBD

4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

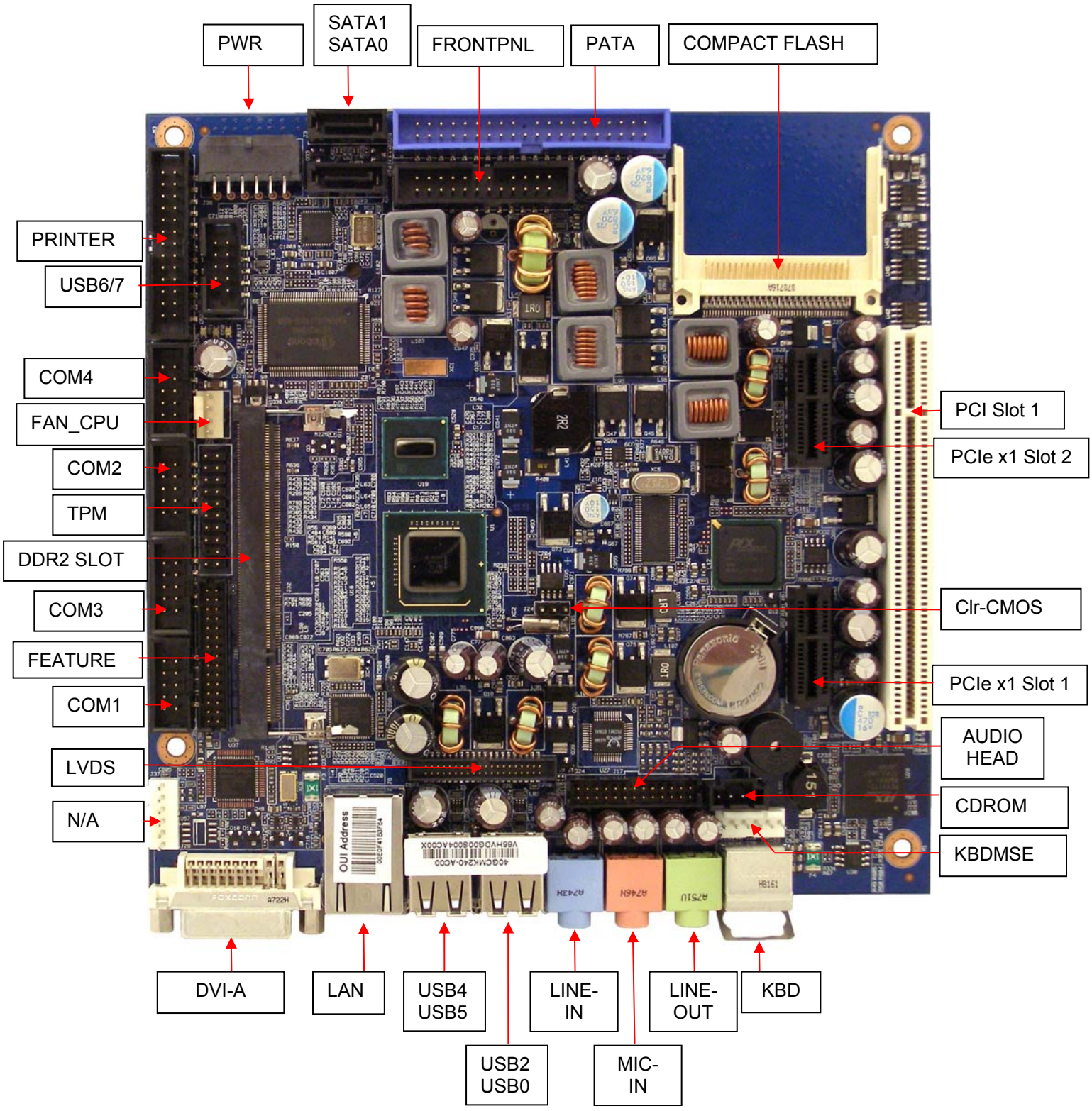
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

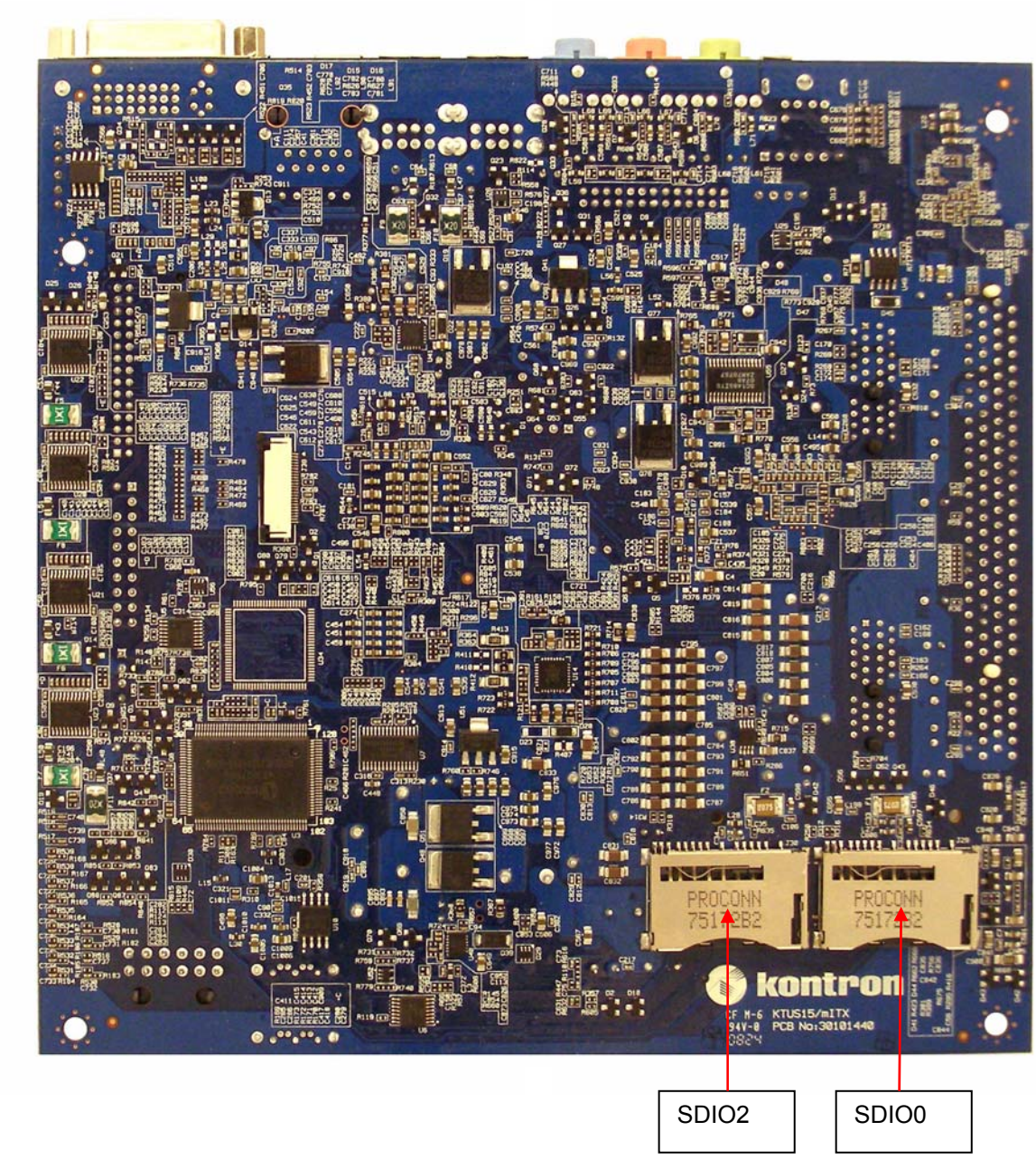
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

4.1.1 KTUS15/mITX, Top-side



4.1.2 KTUS15/mITX, Back-side



4.2 Power Connector (PWR)

The KTUS15 boards are designed to be supplied from a wide-range single supply DC-supply:
5-25V DC +/-5%.

Power Connector, PWR:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	GND	7	1	+Vin	PWR	
	PWR	GND	8	2	+Vin	PWR	
	PWR	GND	9	3	+Vin	PWR	
	PWR	GND	10	4	+Vin	PWR	
	PWR	GND	11	5	+Vin	PWR	
	PWR	GND	12	6	+Vin	PWR	

4.3 Keyboard and PS/2 mouse connectors (KBD)

Attachment of a keyboard or PS/2 mouse adapter can be done through the PS/2 mouse and keyboard connector (KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 MINI-DIN keyboard and mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	2K7	TBD	IOC	MSCLK	6 5	KBDCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
1	2K7	TBD	IOC	MSDAT	2 1	KBDDAT	IOC	TBD	2K7	

Note 1: To use the PS/2 mouse in the KBD connector an adapter cable is required.

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 Keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	2K7	
2	KBDDAT	IOC	TBD	2K7	
3	MSCLK	IOC	TBD	2K7	
4	MSDAT	IOC	TBD	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

4.4 Display Connectors

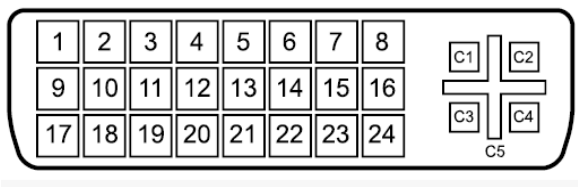
The Intel ® US15W chipset onboard the KTUS15 boards has:

- SDVO channel for display interface
  - SDVO to Analogue / DVI-A (CRT)
  - SDVO to Digital / DVI-D
- LVDS Single channel 18/ 24bit interface

Depending on the KTUS15/mITX board configuration (refer to section KTUS15/mITX Board configurations), the board is either configured for analogue (DVI-A) or digital display (DVI-D) output on the DVI connector. The KTUS15/mITX boards do not support simultaneous analogue and digital output on the DVI connector (DVI-I).

4.4.1 DVI Connector (DVI-A), Analogue output

The **DVI-A** connector only support DVI Analog output. For connecting a standard CRT (analogue) monitor to the DVI-A connector a DVI-CRT adapter can be used (Kontron P/N 822001).



Female socket, front view

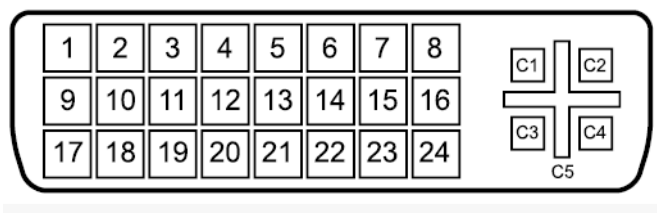
Signal Description - DVI Connector:

Pin No.	Signal	Description	Type	Pull Up	Note
1-5	N.C.		-		2
6	DDC Clock	DDC Clock	IO	2K2	
7	DDC Data	DDC Data	IO	2K2	
8	ANALOG VSYNC	CRT vertical synchronization output.	-		
9-13	N.C.		-		2
14	+5V	Power for monitor when in standby	PWR		1
15	GND		PWR		
16	Hot Plug Detect	Hot Plug Detect	I		
17-24	N.C.				2
C1	ANALOG RED	Analog output carrying the red color signal	O	/75R	
C2	ANALOG GREEN	Analog output carrying the green color signal	O	/75R	
C3	ANALOG BLUE	Analog output carrying the blue color signal	O	/75R	
C4	ANALOG HSYNC	CRT horizontal synchronization output.	O		
C5	ANALOG GND	Ground reference for RED, GREEN, and BLUE	PWR		

Note 1.: The 5V supply is fused by a 1.1A reset-able fuse
Note 2.: DVI digital signals are not supported

4.4.2 DVI Connector (DVI-D), Digital output

The **DVI-D** connector only support DVI Digital output.



Female socket, front view

Signal Description - DVI Connector:

Pin No.	Signal	Description	Type	Pull Up
1	TMDS Data 2-	Digital Red – (Link 1)	LVDS OUT	
2	TMDS Data 2+	Digital Red + (Link 1)	LVDS OUT	
3	TMDS Data 2/4 Shield		PWR	
4	N.C.		-	
5	N.C.		-	
6	DDC Clock	DDC Clock	IO	2K2
7	DDC Data	DDC Data	IO	2K2
8	N.C.		-	
9	TMDS Data 1-	Digital Green – (Link 1)	LVDS OUT	
10	TMDS Data 1+	Digital Green + (Link 1)	LVDS OUT	
11	TMDS Data 1/3 Shield		PWR	
12	N.C.		-	
13	N.C.		-	
14	+5V	Power for monitor when in standby	PWR	1
15	GND		PWR	
16	Hot Plug Detect	Hot Plug Detect	I	
17	TMDS Data 0-	Digital Blue – (Link 1) / Digital sync	LVDS OUT	
18	TMDS Data 0+	Digital Blue + (Link 1) / Digital sync	LVDS OUT	
19	TMDS Data 0/5 Shield		PWR	
20	N.C.		-	
21	N.C.		-	
22	TMDS Clock Shield		PWR	
23	TMDS Clock+	Digital clock + (Link 1)	LVDS OUT	
24	TMDS Clock-	Digital clock - (Link 1)	LVDS OUT	
C1 - C5	N.C.		-	2

Note 1.: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse
Note 2.:DVI analogue signals are not supported

4.4.3 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Pin		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
2K2Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	2K2Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	N.C.	29	30	N.C.	LVDS	
	LVDS	N.C.	31	32	N.C.	LVDS	
	LVDS	N.C.	33	34	N.C.	LVDS	
	LVDS	N.C.	35	36	N.C.	LVDS	
	LVDS	N.C.	37	38	N.C.	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note 1: The KTUS15 board support single channel, 18/24bit OpenLDI/ SPWG?? panels on the LVDS interface up to UXGA (1600x1200??) panel resolution.

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API will be available to operate the BKLTCTL signal. Some Inverters has a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise to the BKLTCTL signal resulting in making the lvds transmision fail (corrupted picture on the display). By adding 1K Ohm resistor in series with this signal and mounted in the Inverter end of the cable kit the noise is limited and picture is stabil.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.

4.5 PCI-Express Connectors

The KT boards contains two 1-lane (x1) PCI Express ports intended for an external PCI Express cards.

The PCI Express port is compliant to the PCI Express* Base Specification revision 1.1.

The two 1-lane (x1) PCI Express ports are supplied through a onboard 5-Lane/5-port PCI express switch.

4.5.1 PCI-Express x1 connector (PCIe x1 Slot 1 and 2)

The KTUS15 boards supports two 1-lane PCI Express (x1) ports.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE CLK		
		PCIE_TXP	B14	A14	PCIE CLK#		
		PCIE_TXN	B15	A15	GND		
		GND	B16	A16	PCIE_RXP		
		NC	B17	A17	PCIE_RXN		
		GND	B18	A18	GND		

4.6 Serial ATA harddisk interface

The KTUS15 boards includes an onboard SATA interface depending on the configuration (refer to section KTUS15/mITX Board configurations).

The SATA Host controller supports 2-port SATA II interface with data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0 and 1.

The board provides two Serial ATA (SATA) connectors, which support one device per connector.
A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

The KTUS15 supports the following RAID (Redundant Array of Independent Drives) levels:
- RAID 0 - data striping
- RAID 1 - data mirroring

Limitations depending on Target Operating System apply.

4.6.1 SATA Hard Disk Connector (SATA0, SATA1)

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

"*" specifies 0, 1 depending on SATA port.

4.7 Parallel ATA harddisk interface

The PATA Host Controller supports three types of data transfers:

- Programmed I/O (PIO): Processor is in control of the data transfer.
- Multi-word DMA (ATA-5): DMA protocol that resembles the DMA on the ISA bus. Allows transfer rates of up to 66 MB/s.
- Ultra DMA: Synchronous DMA protocol that redefines signals on the PATA cable to allow both host and target throttling of data and transfer rates up to 100 MB/s. Ultra DMA 100/66/33 are supported, a 80-wire cable is required.

One parallel ATA harddisk controller is available on the board – a primary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller by means of the 40 pin IDC connector, PATA.

The parallel ATA harddisk controller is shared between the PATA connector and the CF connector.

If the CF connector is not used then two devices (a primary and a secondary device) are supported on the PATA interface.
If the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA device(s).

The signals used for the harddisk interface are the following:

Signal	Description
DAA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCSA1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
DA15..8	High part of data bus.
DA7..0	Low part of data bus.
IORA#	I/O Read.
IOWA#	I/O Write.
IORDYA#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESETA#	Reset signal to the hard disk.
HDIRQA	Interrupt line from hard disk.
CBLIDA	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQA	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACKA#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACTA#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

The pinout of the connectors are defined in the following sections.

4.7.1 IDE Hard Disk Connector (PATA)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESET_P#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.7.2 CF Connector (CF)

This connector is mounted on the topside of the KTUS15/mITX.

The CF socket support DMA/UDMA modules up to UDMA2.

NOTE: If the CF connector is used then only one PATA device is supported and only by use of 40-wire cable (not 80-wire cable). Optionally use SATA device(s). Normally CF is Master and then possible PATA device must be Slave.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	-	-	NC	26	1	GND	PWR	-	-	1
	-	TBD	IO	DA11	27	2	DB3	IO	TBD	-	
	-	TBD	IO	DA12	28	3	DB4	IO	TBD	-	
	-	TBD	IO	DA13	29	4	DB5	IO	TBD	-	
	-	TBD	IO	DA14	30	5	DB6	IO	TBD	-	
	-	TBD	IO	DA15	31	6	DB7	IO	TBD	-	
	-	TBD	O	HDCSA1#	32	7	HDCSA0#	O	TBD	-	
	-	-	-	NC	33	8	GND	PWR	-	-	
	-	TBD	O	IORA#	34	9	GND	PWR	-	-	
	-	TBD	O	IOWA#	35	10	GND	PWR	-	-	
	-	-	PWR	5V	36	11	GND	PWR	-	-	
	8K2	-	I	HDIRQA	37	12	GND	PWR	-	-	
	-	-	PWR	5V	38	13	5V	PWR	-	-	
	-	-	PWR	GND	39	14	GND	PWR	-	-	
	-	-	-	NC	40	15	GND	PWR	-	-	
	-	TBD	O	RESET_C#	41	16	GND	PWR	-	-	
	4K7	-	I	IORDYA	42	17	GND	PWR	-	-	
	-	-	I	DDRQA	43	18	DAA2	O	-	-	
	-	-	O	DDACKA#	44	19	DAA1	O	-	-	
	-	-	I	HDACTA#	45	20	DAA0	O	-	-	
	-	-	I	CBLIDA#	46	21	DB0	IO	TBD	-	
	-	TBD	IO	DB8	47	22	DB1	IO	TBD	-	
	-	TBD	IO	DB9	48	23	DB2	IO	TBD	-	
	-	TBD	IO	DB10	49	24	NC				
1	-	-	PWR	GND	50	25	NC	-	-	-	2

Note 1: Pin is longer than average length of the other pins.
Note 2: Pin is shorter than average length of the other pins.

4.8 Printer Port Connector (PRINTER).

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode.

4.9 Serial Ports

Two or four RS232 serial ports are available on the KTUS15 boards depending on the configuration (refer to section KTUS15/mITX Board configurations).

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.9.1 Com1, 2, 3, 4 Pin Header Connector.

The pinout of Serial ports Com1, 2, 3 and 4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: The COM 1, 2, 3 and 4 header 5V supply is fused with individual 1.1A resetable fuses for each connector.

A DB9 adapter (ribbon cable) is available for connecting the COM ports to I/O front panel.

4.10 Ethernet connectors.

The KTUS15 board support 1 channel of 10/100/1000Mb Ethernet using the Intel® 82574L PCI express LAN controller.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[0]-	
MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[1]-	
MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]-	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]-	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

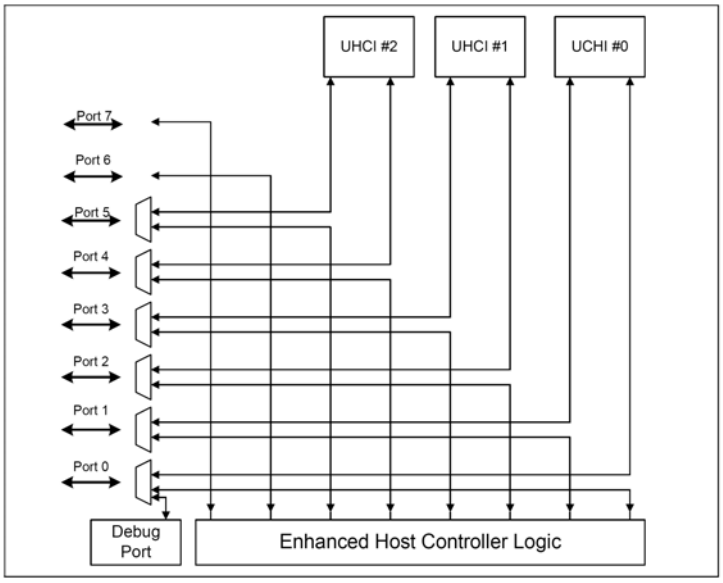
4.10.1 Ethernet connector (LAN)

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

4.11 USB Connector (USB)

The KTUS15 boards contains three Universal Host Controller Interface (UHCI) USB 1.1 controllers and an Enhanced Host Controller Interface (EHCI) USB 2.0 controller.



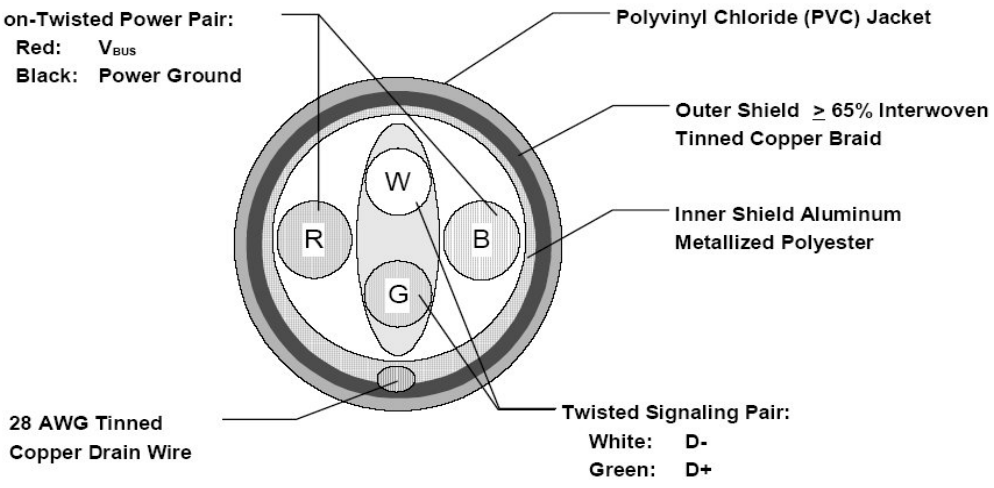
A total of eight USB ports are supported. All eight of these ports are capable of highspeed data transfers up to 480 MB/s, and six of the ports are also capable of full-speed and low-speed signaling (USB Ports 0, 1, 2, 3, 4, 5).

The KTUS15 boards supports USB client functionality on port 2 of the USB interface. This permits the platform to attach to a separate USB host as a peripheral mass storage volume or RNDIS device.

USB Legacy mode is supported. Over-current detection on all eight USB ports is supported.

USB Port 0 and 2 are supplied on the combined USB0, USB2 connector.
USB Ports 1 and 3 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.
USB Port 4 and 5 are supplied on the combined USB4, USB5 connector.
USB Port 6 and 7 are supplied on the USB6, USB7 internal pinrow connector.

Note: It is required to use only High-/Full-Speed USB cable, specified in USB2.0 standard:



4.11.1 USB Connector 0/2 (USB0/2)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.

Signal	Description
USB0+ USB0- USB2+ USB2-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.11.2 USB Connector 4/5 (USB4/5)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

4.11.3 USB Connector 6/7 (USB6/7)

USB Ports 6 and 7 are are supplied on the internal USB6, USB7 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB6-	3	4	USB7-	IO		-	
	-		IO	USB6+	5	6	USB7+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 2.0A reset-able fuse.

Note 1: The 5V supply for the USB devices is on-board fused with a 2.0A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.

4.12 Audio Connector

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio, featuring ten 24-bit stereo DACs and two 20-bit stereo ADCs.
The Audio signals are made available on the Frontpanel connectors (Line in / Line out / MIC) and the onboard AUDIO_HEAD and CDROM Audio input connectors.

4.12.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the audio jack connectors.

	Signal	Type	Note
TIP	LINE1-IN-L	IA	1
RING	LINE1-IN-R	IA	1
SLEEVE	GND	PWR	

	Signal	Type	Note
TIP	MIC1-L	IA	1
RING	MIC1-R	IA	1
SLEEVE	GND	PWR	

	Signal	Type	Note
TIP	LINE-OUT-L	OA	
RING	LINE-OUT-R	OA	
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

Signal descriptions

Signal	Description	Note
LINE-OUT / FRONT	Line out / Front Speakers	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	

4.12.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

4.12.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

4.13 Fan connectors, (FAN_CPU)

The **FAN_CPU** is used for connection of the FAN for the CPU or System.

The 4pin header supports connection of 3-pin FANs, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is controlled in the BIOS setup menu.

4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	4K7	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

3-pin Mode:

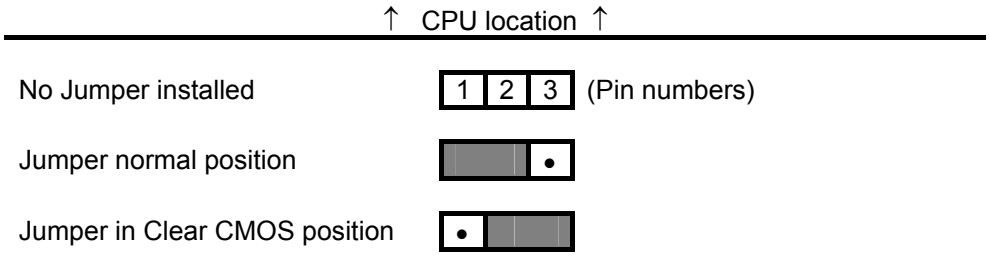
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
-	-	-	-	-	
2	SENSE	I	-	4K7	
3	+12 V	PWR	-	-	
4	GND	PWR	-	-	

Signal description:

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000 mA can be supplied from this pin.
GND	Power Supply GND signal

4.14 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.



To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute. With the jumper in Clear CMOS position, any Secure CMOS settings will also be void.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

4.15 TPM connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	NC				

4.16 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	NC	9	10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
1				MIC2-L	23	24	MIC2-R				1

Note 1: Unsupported inputs, leave these inputs unconnected.

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connectorfladkabel or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for minimum 16mS the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R are unsupported. Leve these terminals unconnected.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

4.17 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I		4K7	3
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	4K7/	1
	-	-	PWR	GND	19	20	FAN3OUT	O		4K7	3
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	4K7/			SMBC	29	30	SMBD			4K7/	1

Note 1: Pull-up to +3V3Dual (+3V3 or SB3V3). Note 2: Pull-up to onboard Battery. Note 3: Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC. Current draw is 3-4µA when PSU is disconnected.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for WinXP and Win2000.
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be set to output voltages from 0 – 3V3 to control the Fan's speed.. For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref). (Precision +/- 3ºC)
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

4.18 PCI Slot Connector (PCI Slot 1)

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE				**COMPONENT SIDE**			
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.18.1 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.18.2 KTUS15 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
KTUS15/mITX	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD30, INT_PIRQ#D, INT_PIRQ#A, INT_PIRQ#B, INT_PIRQ#C.

5. Onboard Connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_CPU	Foxconn	HF2704E-M1	AMP	1375820-4 (4-pole)
	AMP	1470947-1	AMP	1375820-3 (3-pole)
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA0-1	Molex	67491-0020	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
PWR	Molex	43045-1201	Molex	43025-1200
			Kontron	KT 1022-6309 (cable kit for ATX)
COM1, 2, 3, 4	Foxconn	HL20051	Molex	90635-1103
			Kontron	KT 821016 (cable kit)
			Kontron	KT 821017 (cable kit)
USB1 USB3 (*)	(FRONTPNL)	-	Kontron	KT 821401 (cable kit)
PRINTER	Foxconn	HL2213F	Molex	90635-1263
			Kontron	KT 821031 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Foxconn	HL20121	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)

* USB1/USB3 are located in FRONTPNL connector. Depending on application the KT821401 can be used.

6. System Ressources

6.1 Memory map

Address range (hex)	Size	Description

6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function

6.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Parallel Port	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used for SATA RAID controller	May be used for onboard Sound System	May be used for PCI Express Root Port	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQD depending on selections in the BIOS	Notes
NMI																				
IRQ0																				
IRQ1																				
IRQ2																				
IRQ3																				
IRQ4																				
IRQ5																				
IRQ6																				
IRQ7																				
IRQ8																				
IRQ9																				
IRQ10																				
IRQ11																				
IRQ12																				
IRQ13																				
IRQ14																				
IRQ15																				
IRQ16																				
IRQ17																				
IRQ18																				
IRQ19																				
IRQ20																				
IRQ21																				
IRQ22																				
IRQ23																				
IRQ24																				
IRQ25																				
IRQ26																				

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ26 are APIC interrupts

6.4 I/O Map

Address (hex)	Size	Description

Notes:

6.5 DMA Channel Usage

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

7. Overview of BIOS features

This Manual section details specific BIOS features for the KTUS15 boards.
The KTUS15 boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

7.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

7.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

8. BIOS Configuration / Setup

8.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KTUS15 board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit

The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in bold, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

8.2 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

9. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTUS15 Driver CD or they can be downloaded from the homepage http://www.kontron.com/

Note: When installing Intel ® Graphics drvers it is possible that the OS start up without any connected display(s) active. If you are able to pass the "Log On to Windows" etc. by entering the password etc. without actually see the picture on the display and If the Hot Keys have not been disabled in the Extreme Graphic driver then the following key combinations you can select a connected display:

<Ctrl><Alt><F1> enables the sDVO channel which controls the DVI-D or DVI-A display output depending on board configuration. Refer to configuration overview: KTUS15/mITX Board configurations for details.

10. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.